REMARKS/ARGUMENTS

Claims 1-3, 5-6, 8-9, and 12-21 were previously pending in the application. Claim 21 is canceled herein. Assuming the entry of this amendment, claims 1-3, 5-6, 8-9, and 12-20 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

On page 2 of the office action, the Examiner rejected claims 18 and 20-21 under 35 U.S.C. 102(b) as being anticipated by Jelinek. On page 3, the Examiner allowed claims 1-3, 5-6, 8-9, and 12-17 and objected to claim 19 as being dependent upon a rejected base claim, but indicated that claim 19 would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all of the now-pending claims are allowable.

Claim 18 is directed to a voltage-controlled oscillator comprising (a) a set of interconnected delay stages and (b) switch-controlled load circuitry connected to the output of one or more delay stages. The switch-controlled load circuitry includes a transistor, a switch connected between a delay stage output and a gate node of the transistor, and a current source connected between a power supply for the transistor and a channel node of the transistor.

Fig. 2 shows an exemplary embodiment of the invention of claim 18 in which:

- Transistor 204ap is an example of the transistor of claim 18;
- Switch 206ap is an example of the switch of claim 18; and
- Current source 208ap is an example of the current source of claim 18; and
- vdd is an example of the power supply of claim 18.

As shown in Fig. 2, switch 206ap is connected between output OUTP of delay stage 202a and the gate node of transistor 204ap.

In rejecting claim 18, the Examiner cited the circuitry of Fig. 2F of Jelinek as providing an example of the switch-controlled load circuitry of claim 18. In particular, the Examiner stated that "Fig. 2F shows a switch (680 or 690) connected between a delay stage output ("01 TO FIG.2F" see Fig. 2C) and gate node of the transistor (PMOS 681, 682)." For the following reasons, the Applicant respectfully submits that the Examiner mischaracterized the teachings in Jelinek in rejecting claim 18.

The Examiner correctly identifies line 01 as corresponding to an output of a delay stage. See Figs. 2A and 2C. In addition, transistors 680 and 690 are connected to operate as switches. However, the Examiner mischaracterized transistors 680 and 690 as being connected between a delay stage output and the gate node of a transistor. As clearly shown in Fig. 2F, transistor 680 is connected between power supply V_{dd} and channel nodes of transistors 681 and 682, while delay stage output line 01 is connected directly to the gate node of transistor 681. Similarly, transistor 690 is connected between power supply V_{dd} and channel nodes of transistors 691 and 692, while delay stage output line 01B is connected directly to the gate nodes of transistors 682 and 691. Thus, neither transistor 680 nor transistor 690 is connected between a delay stage output and the gate node of a transistor.

In view of the foregoing, the Applicant submits that the Examiner mischaracterized the teachings in Jelinek and improperly applied those mischaracterized teachings to reject claim 18. As such, the Applicant submits that the rejections of claims 18 and 20 are improper and should be withdrawn.

For all these reasons, the Applicant submits that claim 18 is allowable over Jelinek. Since claims 19 and 20 depend from claim 18, it is further submitted that those claims are also allowable over Jelinek. The Applicant submits therefore that the rejections of claims under Section 102(b) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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